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CENTRAL FAX CENTER****DEC 02 2005****Amendment to the Abstract:**

Please cancel the previous abstract and replace it with the following abstract:

A method and system for testing an embedded DRAM that includes DRAM blocks. The method including: generating a test data pattern in a processor based BIST system, for each DRAM block, performing a write of the test data pattern into the DRAM block, performing a pause for a predetermined period of time, and performing a read of a resulting data pattern from the DRAM block; where for each DRAM block, the write of the test data pattern into the DRAM block is performed before the pause, and the read of the resulting data pattern from each DRAM block is performed after the pause; where at least a portion of the pause of two or more of the DRAM blocks overlap in time; and for each DRAM block comparing the test data pattern to the resulting data pattern.